### MASSACHUSETTS INSTITUTE OF TECHNOLOGY

Department of Electrical Engineering and Computer Science

# 6.301 Solid State Circuits

Fall Term 2010	Issued : November 5, 2010
Design Problem	Due : Friday, December 3, 2010

Work independently. Consultation with the 6.301 staff and other inanimate objects is encouraged. You are not required to build your design, but computer verification of your final design is required. Read this handout thoroughly.

### **Project:**

Design a transimpedance amplifier. Minimum specifications include:

open-loop transimpedance at d-c with a $1 \mathrm{k} \Omega$ load	$> 200 \mathrm{k}\Omega$
input common mode and output range	$\pm 10 V$
output current	$\pm 10 \mathrm{mA}$
power supply voltages	$\pm 15 V$
quiescent power consumption	$< 250 \mathrm{mW}$
transistors	see SPICE models below

Use the topology below, with the bias current  $I \ge 1$ mA. Bias all transistors used in the buffer amplifiers at  $I_C \approx 1$ mA.



You may have to use a mirror that has an output resistance greater than  $r_o$  and an output buffer with a current gain of  $\beta^2$  to meet specifications.

# 1 Assignment:

There are two options for this assignment: you may either simulate your design in SPICE, or build it. Note that construction is not required for this project, and that either option will be graded with equal weight.

# 1.1 OPTION 1: Simulation

For this option, use the SPICE models below. You may use ideal current sources for biasing. Work out a preliminary design based upon typical numbers from the transistor models. Analyze the circuit by hand, making reasonable approximations. In your report, convince us that you understand this topology. Show that your design meets the specifications listed above. Then connect your design as shown below.



The transfer function  $\frac{v_o}{v_i}(j\omega)$  has an angle of  $-180^\circ$  at low frequencies, and the angle becomes more negative as frequency increases. Determine a value for R that results in an angle of  $-225^\circ$  when the  $|\frac{v_o}{v_i}(j\omega)| = 1$ (that is, results in a phase margin of  $45^\circ$ ).

Then connect your amplifier as shown to get a nominal closed loop gain of 11.



What is the bandwidth of your amplifier in this connection? What is the actual closed-loop gain at low frequencies?

Your report should be short and informal. Include appropriate plots to support that your design meets all specifications.

### Transistor models:

```
* Q[name] Nc Nb Ne [model name]
```

```
.model npn1 npn is=15fA bf=200 vaf=50 cje=10p tf=750p cjc=1p
.model pnp1 pnp is=15fA bf=50 vaf=25 cje=10p tf=750p cjc=1p
```

## **1.2 OPTION 2: Construction**

For this option, you are not required to simulate your design.

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