

Massachusetts Institute of Technology
Department of Electrical Engineering and Computer Science

6.976
High Speed Communication Circuits and Systems
Spring 2003

Homework #2: High Speed Amplifiers

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Reading: Chapters 3 and 8 and pages 280-283 of Thomas H. Lee's book.

1. The following is based on Problem 8 in Chapter 8 of Thomas Lee's book. Consider the zero-peaked amplifier shown in Figure 1.

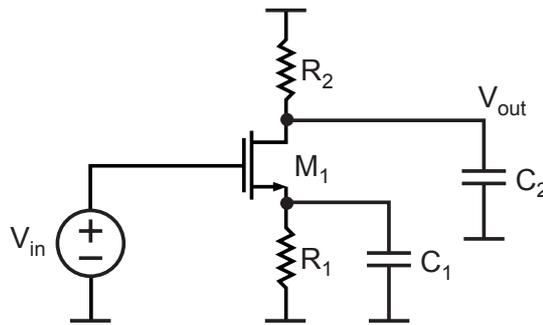


Figure 1: Zero-peaked amplifier.

- (a) Derive the transfer function expression for the small-signal gain from V_{in} to V_{out} . In your derivation, assume that M_1 is in saturation, and ignore C_{gd} , r_o , and backgate parasitics.
- (b) Express the bandwidth of the amplifier as a function of the output pole, $1/(R_2C_2)$, under the assumption that $g_mR_1 = 9$ and C_1 is chosen such that the zero cancels the output pole in the gain expression derived above. Recognize that the output pole frequency corresponds to the bandwidth of the *unpeaked* amplifier.
2. The following is based on Problem 7 in Chapter 8 of Thomas Lee's book. In general, high-speed followers, as shown in Figure 2, have a tendency to ring or even oscillate when driving certain loads. Your task is to identify the conditions that may cause this problem and to propose a solution. For derivations, ignore C_{gd} , r_o , and backgate parasitics of M_1 .
- (a) Consider the follower circuit in part (a) of the figure. Derive an expression for Z_{in} .

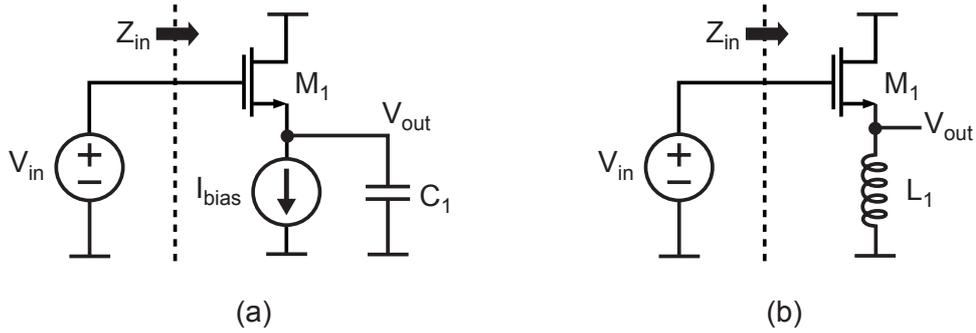


Figure 2: Source follower with a (a) capacitive load, (b) inductive load.

- (b) Over what range of load capacitance can the real part of Z_{in} , as derived above, be negative? What is the impact of having the real part of the impedance become negative?
- (c) Given that the load capacitance is chosen such that the real part of Z_{in} becomes negative, modify the circuit in part (a) of the figure such that the source V_{in} always sees an impedance whose real part is positive. In your design, be sure to preserve the high speed operation of the follower circuit, and provide formulas for the computation of the values of any components you add.
- (d) Now consider the follower circuit with an inductor load in part (b) of the figure, whose analysis will also provide intuition of the impact of inductive source degeneration on CE and CS circuits. Derive an expression for Z_{in} under the assumption that C_{gd} and r_o of M_1 can be ignored. Examining the real part of the derived impedance, comment on whether ringing or oscillation problems can occur.
3. This problem will focus on the design of the narrowband amplifier shown in Figure 3. Assume that all devices are the same size with width of 100 microns and length of 0.18 microns. For all hand calculations, ignore C_{gd} , r_o , backgate effects, and overlap for all transistors.

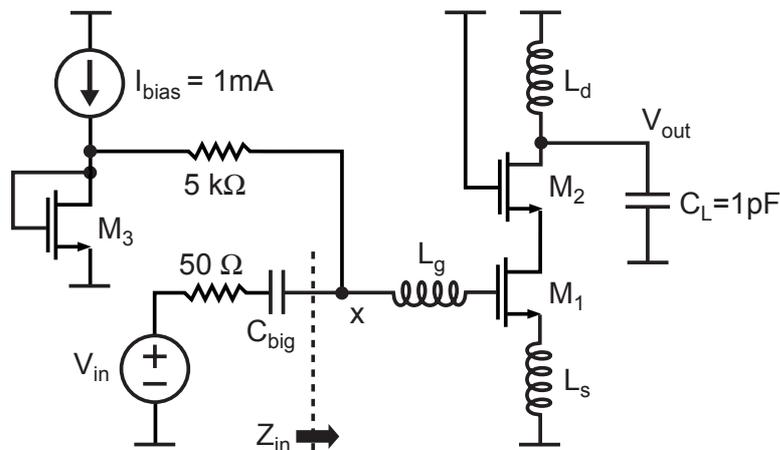


Figure 3: A high speed, tuned cascode amplifier.

- (a) Compute C_{gs} and g_m for all the transistors at the operating point set by the bias configuration shown in the figure. Be sure to determine these parameters “by hand” based on the transistor parameters contained in the 0.18u Hspice model file provided on Athena in the file /mit/6.976/Models/0.18u/mos018.mod. For all parts to follow, use C_{gs} and g_m from Hspice and also include the appropriate C_{db} .
 - (b) Given that the Q of all of the inductors at 10 GHz is 5, determine L_s , L_g , and L_d to achieve 50 Ohm input impedance (Z_{in}) and maximum gain (V_{out}/V_{in}) at 10 GHz. Use a simple inductor model of a resistor in series with an inductor. State the maximum gain that you achieved.
 - (c) Repeat part (b) given that the Q of all of the inductors at 10 GHz is 20. How does the maximum gain change?
 - (d) Build the two circuits from (b) and (c) in Cadence on Athena and use Hspice and Matlab to plot Z_{in} (real and imaginary parts) and the amplifier gain (V_{out}/V_{in}) over the frequency range of 1 GHz to 20 GHz.
 - (e) Using Hspice and Matlab, compute and plot $|S_{11}|$ and $|S_{21}|$ over the frequency range of 1 GHz to 20 GHz for both circuits in (d). For these exercises, assume that the input of the two-port is node x , and that the output is V_{out} .
4. This problem focuses on the design of the broadband differential amplifier shown in Figure 4 based on the techniques described in class. Perform all computations based on the transistor models contained in the 0.18u Hspice model file provided on Athena in the file /mit/6.976/Models/0.18u/mos018.mod. For simplicity, assume all devices are the same size with transconductance g_m , all resistors are of the same value R , and that C_{fixed} , which corresponds to wiring capacitance, equals 15 fF.

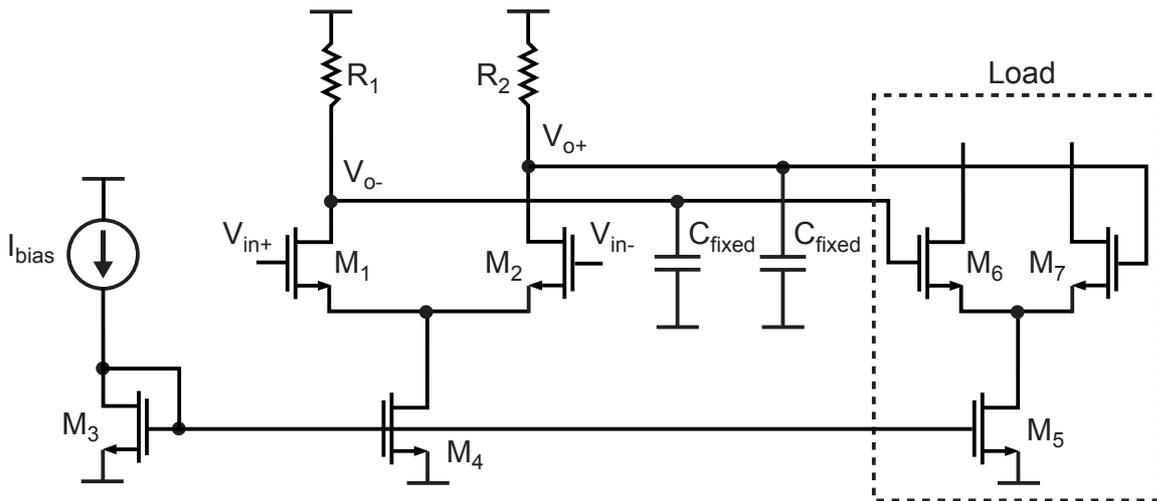


Figure 4: A high speed differential amplifier.

- (a) Using Hspice and Matlab, plot the g_m versus I_d curve for a diode-connected NMOS device of width 2.0 microns and length 0.18 microns. The value of I_d should span

from 0 to the value produced when V_{gs} equals 1.8 V. Use Hspice LX7() function to extract g_m from simulation.

- (b) Compute the value of C_{gs} for the transistor in part (a) under the assumption that the NMOS device is in saturation.
- (c) Write a Matlab script that determines the value of I_d at which the g_m curve generated in part (a) intersects with the line $(A/V_{sw})I_d$, where A corresponds to the single-ended amplifier gain ($g_m R$), and V_{sw} corresponds to the single-ended amplifier swing ($I_{bias} R$). State the value of I_d that results with $A = 5$ and $V_{sw} = 1$ V.
- (d) Based on the results in part (c), compute the bandwidth of the amplifier for the case where $A = 5$ and $V_{sw} = 1$ V under the restriction that the device size has a width of 2 microns and a length of 0.18 microns.
- (e) Based on the results in part (c), what is the maximum bandwidth that can be achieved for $A = 5$ and $V_{sw} = 1$ V when the device size can be arbitrarily set? What is the penalty to achieving the maximum bandwidth?
- (f) In practice, a good compromise is to size the amplifiers such that their input load capacitance, i.e., C_{gs} , equals the fixed capacitance. Given this constraint, what is the appropriate device width and length, resistor load value R , and resulting bandwidth to achieve $A = 5$ and $V_{sw} = 1$ V?
- (g) Based on the insight gained in this problem, write a Matlab script that determines the maximum gain that can be achieved with a single-stage amplifier bandwidth of 2.5 GHz, 5 GHz, and 10 GHz. Assume that the devices are sized according to the constraint specified in part (f), and that $V_{sw} = 1$ V. State the values of gain that you achieve at each bandwidth setting.